AMM1A
Master Analog Measurement Module

The AMM1A Analog Measurement Module combines three important Series 500 functions into a single module. First, the AMM1A functions as a standard analog input module, and will accept up to 16 single-ended or eight differential analog input signals. It contains signal conditioning and switching circuitry for these channels. Second, the AMM1A selects and conditions analog signals from other analog input modules in a Series 500 system. Last, the AMM1A serves as a 12-bit A/D converter for its own analog input channels, as well as any other analog signals which have been processed by the global select/conditioning circuitry. After analog conditioning, signals are routed to the A/D converter section of the module for the analog-to-digital conversion process.

Input signals are applied to the AMM1A's analog input channels through on-card quick-connect screw terminals. The AMM1A has a total of 16 local single-ended, or eight differential inputs. The input configuration is controlled through software, rather than with hardware switches. These analog input channels can be conditioned with programmable local gains of either x1 or x10.

Global conditioning consists of a high-speed software-controlled gain amplifier with programmable x1, x2, x5 and x10 gain values. All analog inputs connected to the Series 500 pass through the global circuitry, whether the signals originate on the AMM1A or some other analog input module. Therefore, these gain values can be applied to any analog input in the system.

For A/D conversion, the AMM1A uses a 12-bit successive approximation converter. A maximum conversion time of only 16μsec allows sampling rates as high as 62.5kHz. to maximize resolution, the AMM1A has 0-10V and ±10V A/D converter ranges which are software selectable.

CAUTION: Always turn off the system power before installing or removing modules. To minimize the possibility of EMI radiation, always operate the system with the top cover in place and properly secured.

The AMM1A is designed to be used only in slot 1 of the 500-series chassis, Model 575, or Model 576. To install the module in a series 500 chassis, first remove the baseboard top cover and install the module in slot 1 with the component side facing the power supply. For Model 575 or 576, please refer to the Set-up section of its hardware manual.

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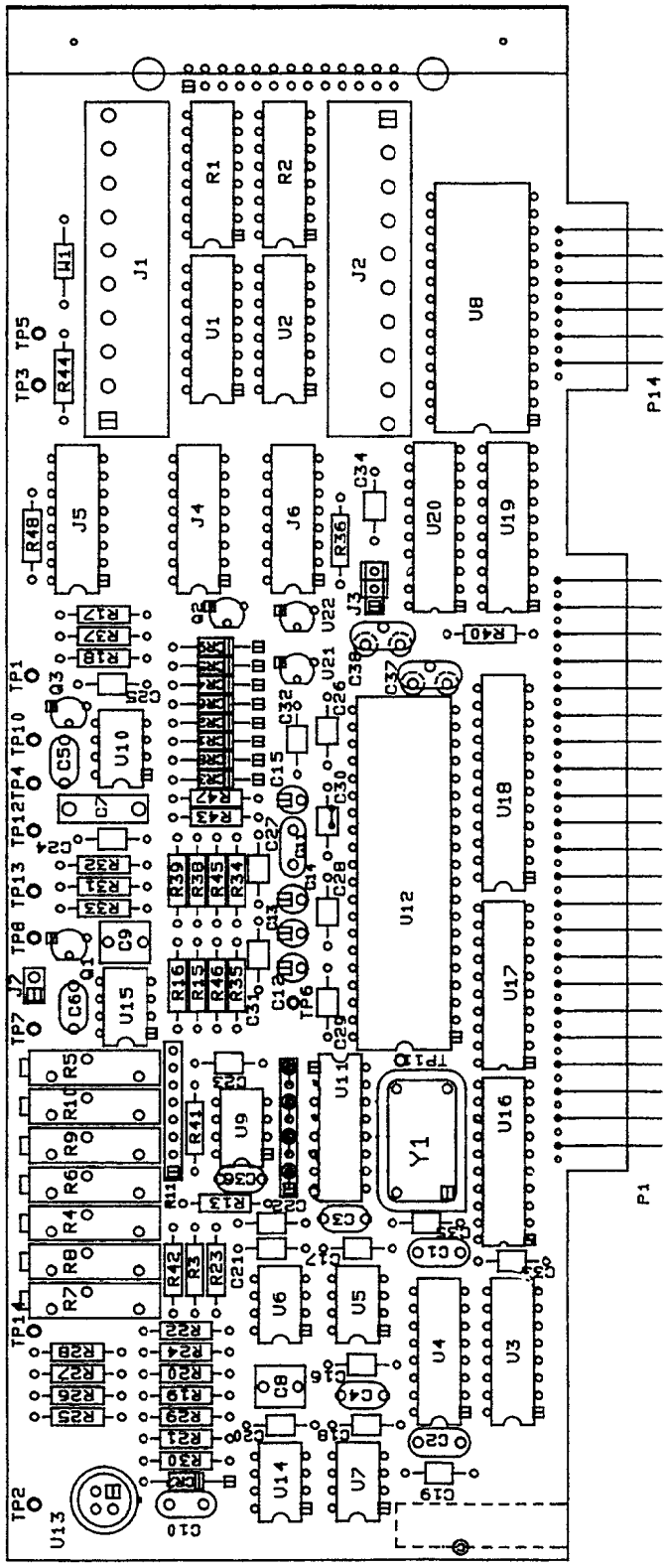
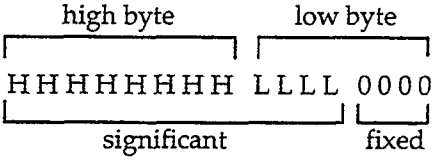


Figure 1. AMM1A Component Layout

SOFTWARE CONSIDERATIONS THE AMM1A ANALOG MODULE

The AMM1A module, when used in a 575 or 500 series chassis, operates with KDAC500 and a variety of 3rd party software packages. For programmers who are writing their own register level driver, the following data format explanation is provided:

BASIC PEEK/POKE operations and equivalent commands in other programming languages must access the AMM1A as a 16-bit A/D module, rather than a 12-bit module. The AMM1A's 12-bit resolution results from padding the last four of the 16 bits with zeros. The least significant bit position where change will be observed in the fifth least significant bit, and the low byte will increment by 1000 binary. The high and low bytes carry information as follows:



where: H = high-order bit (8)
L = low-order bit (4)
0 = bit permanently wired low (4)

Thus, a complete read of the AMM1A requires that a high and low byte be read. Converting the high and low bytes to a full A/D count can be performed as follows:

RES = (256 * HIBYTE) + LOWBYTE

The equivalent voltage can be calculated by multiplying RES by the bit value for a 16-bit conversion referenced to the A/D converter range. Consult the following examples:

Assume a decimal value for HIBYTE of 170, and 48 for LOWBYTE. RES can be calculated as:

RES = 170*256 + 48
RES = 43568

1. For an A/D range of ±10 volts, calculate the corresponding voltage reading as:

   V = (RES * 20/65536) - 10
   V = (43568 * 20/65536) -10
   V = 3.296V

2. For an A/D range of 0-10 volts, calculate the corresponding voltage reading as:

   V = (RES * 10/65536)
   V = (43568 * 10/65536)
   V = 6.648

AMM1A High-speed Acquisition Mode with the ANINQ Command (KDAC500)

The ANINQ command can operate the AMM1A module in a high-speed "auto-acquire" mode at an aggregated throughput rate of up to 62.5kHz. Auto-acquire applies to single or multiple channels. For multiple channels, the per-channel scan rate equals 62.5kHz divided by the number of channels.

The analog input modules AIM2 and AIM3A can also provide up to 62.5kHz throughput when these modules are used in a system containing an AMM1A.

To operate the AMM1A in auto-acquire mode, you must satisfy the following requirements:

1. The analog input channels sampled by ANINQ must be on an AMM1A, AIM2, or AIM3A.
2. All channels sampled by the specific ANINQ command must be on one module.
3. The AMM1A's input filter must be set to 100kHz.

If any of these conditions cannot be met, the speed of an ANINQ command will revert to the speed of a BGREAD command. Under these circumstances, it is better to use BGREAD in order to take advantage of foreground/background operating mode.

NOTE: The ANINQ command in KDAC500 has been optimized for auto-acquire operation with the AMM1A. If you attempt auto-acquire mode with BASIC's PEEK/POKE, or the memory READ/WRITE commands of other languages, you may receive incorrect data. If you do not use KDAC500, Keithley suggests that you run the AMM1A only in "regular acquisition mode". This mode is described under the heading "SELECT ACQUISITION MODE" later in this manual.

Self-calibrating During "CALL KDINIT" (KDAC500)

The AMM1A module performs a calibration of the A/D gain and range each time KDINIT is called. KDAC500 executes the KDINIT function automatically each time it is loaded. KDAC500 will expect an AMM1A module in the system if the configuration file (CONFIG.TBL) shows an AMM1A in slot 1. If the software cannot complete the calibration, it will issue an error message such as "Unable to calibrate A/D module". If this occurs, check that:

1. The data acquisition hardware is turned on.
2. The cable between the hardware and the host computer is connected.
3. An AMM1A module is mounted in slot 1 of the data acquisition system

Connection and Operation

Signal Connection

The AMM1A can be programmed for either differential or single-ended local input configurations. These local input signals are applied to screw terminals located toward the rear portion of the AMM1A. Single-ended and differential inputs use the same screw terminals.

The channel numbers are shown in Figure 1. Figure 2 shows typical connections for channels 0 through 7 in differential mode. For differential mode, connect the high (+) side of an input signal to the (+) terminal, and the low (-) side of the signal to the corresponding (-) terminal. When the AMM1A is configured for single-ended input, connect the high (+) side of the input signal to one of the terminals 0 through 15, and the low (-) side to the module ground at either end of the terminal strip. In Figure 2, the numbers listed in parentheses above the lower connector are the single-ended local channels 9 through 15.

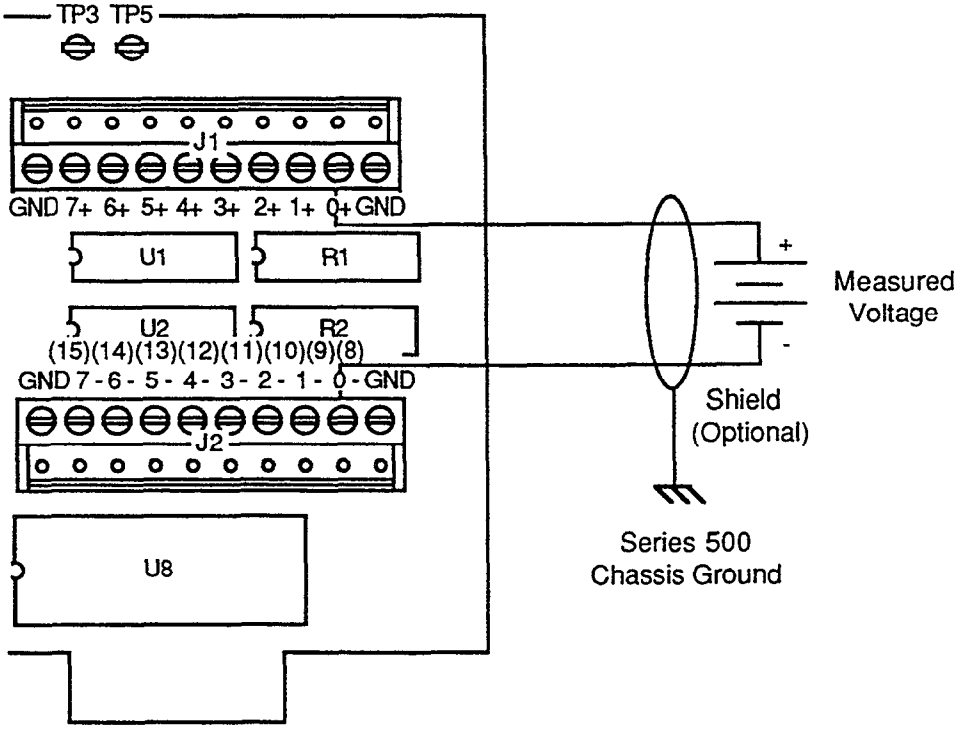


Figure 2. Typical Differential Connection (Channel 0 Shown)

CAUTION: The AMM1A inputs are non-isolated. In single-ended mode, one side of the input is connected to power line ground. Any signal connected to the AMM1A must also be referenced to power line ground, or module or system damage may occur. Also note that inaccuracies on other channels may result. When used in differential mode, the AMM1A local inputs must both be within ±10V of module ground for proper operation. If either signal exceeds ±30V module damage may result.

In many situations, shielded cable may be required to minimize EMI radiation, or to keep noise to a minimum. If shielded cable is used, connect the shield to ground only, and do not use the shield as a signal-carrying lead. Usually, a module ground terminal should be used, but in some cases better results may be obtained by using one of the baseboard ground posts. Use the configuration that results in the lowest noise.

For shielding to be effective, the shield must contain both high and low signal wires, and must not carry any other signals. If a number of AMM1A signal input lines are shielded, all shields should be connected to the same ground terminal.

Signal Conditioning

Figure 3 shows a simplified block diagram of the AMM1A. The module is divided into six general sections: a local multiplexer, a local programmable gain amplifier, a global multiplexer, a global programmable gain amplifier, a programmable low-pass filter, and a 12-bit A/D converter.

Local input signals from channels 0 to 15 are applied to the local multiplexer for selection. At any given time, only one channel will be selected, as determined by the SELECT CHANNEL command (covered later in this section). The signal from the selected channel is then routed through a local programmable gain amplifier to the global multiplexer for further signal selection and conditioning.

The global multiplexer selects a single signal from among the 10 slots in the 500 series chassis. In this manner, signals from any of the 10 slots can be selected by software. The global multiplexer is controlled by the SELECT SLOT command, discussed later in this section. Users of the 575 or 576 should consult its hardware manual for information on how the global multiplexer selects signals from slot 3 and from the 3B channel connector.

After the signal is selected, the Global PGA applies software-selectable gains of x1, x2, x5, or x10. The signal finally passes through a one-pole filter with software selectable -3db frequencies of either 100kHz or 2kHz. When this signal conditioning process is complete, the signal is routed to the 12-bit A/D converter for digitization. After the conversion process, digital data representing the applied signal travels via the baseboard and interface card to the host computer.

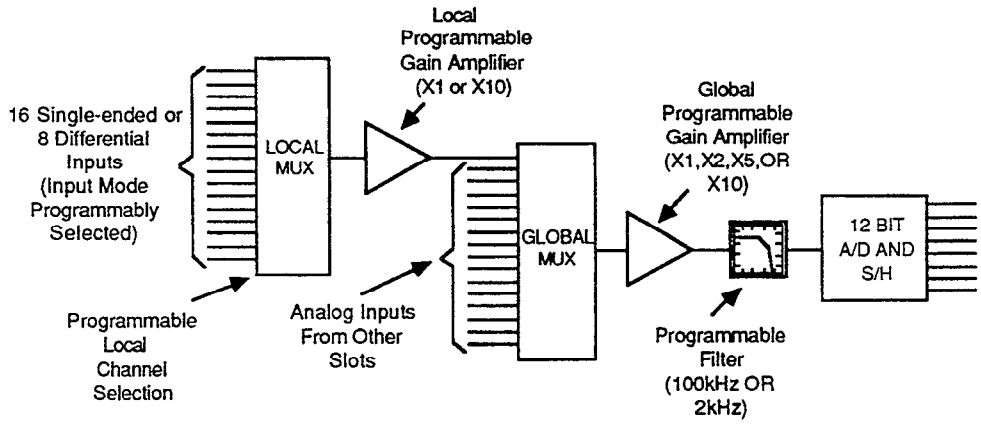


Figure 3. AMM1A Signal Conditioning

Input Filtering

Noise introduced into the input signal can corrupt the accuracy of the measurement. Such noise will usually be seen as an unsteady reading, or, in some cases, as a constant offset. In the former case, the effects of noise will usually be quite obvious, but may not be noticeable in the steady-state offset situation.

Frequently, noise is introduced into the signal from 50 to 60Hz power sources. In many cases, noise can be attenuated by shielding or relocating the input signal lines, as discussed earlier. It may also be possible to reject unwanted 60Hz noise by using the AMM1A in differential mode. Since the 60Hz noise may also be present on the low side of the signal, the differential amplifier will reject the common signal. In more difficult situations, however, it may be necessary to filter the input signal to achieve the necessary noise reduction.

When noise is a problem, a single-pole low-pass filter like the one shown in Figure 4 can be connected between the input signal and the corresponding AMM1A channel. Note that the filter is made up of a single capacitor and resistor with the capacitor connected between the AMM1A channel input terminals and the module ground terminal. The resistor is then placed in series with the high input signal lead.

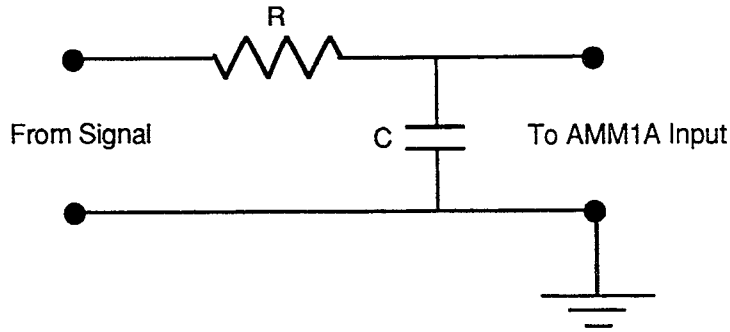


Figure 4. Input Filtering

A common reference point for a simple filter like the one in Figure 4 is the -3dB or half-power point, which is given as follows:

$$f_{-3dB} = 1/(2\pi RC)$$

where f is in Hz, C is in farads, R is in ohms. Above this frequency, filter response will roll off (decrease) at a rate of -20dB per decade. Thus, each time the frequency increases by a factor of 10, filter output voltage decreases by a factor of 10 (-20dB).

Although such filtering can quiet down a noisy signal, there is a trade-off in the form of slower response. This response time may be important in the case of a rapidly changing input signal. For the filter in Figure 4, the response time to 1% of final value is 4.6RC, while the response times to 0.1% and 0.01% of final value are 6.9RC and 9.2RC, respectively.

As a example, assume that 10 counts of 60Hz noise is present in the input signal. To reduce the noise to one count, an attenuation factor of 10 (-20dB) at 60Hz will be necessary. Thus, the filter should have a -3dB point of 60Hz.

To determine the relative RC values, the above equations can be rearranged to solve for either R or C. If we wish to choose a nominal capacitor value and then solve for the resistance, we have:

$$R = 1/(2\pi C f_{-3db})$$

Choosing a nominal value of 2μF for C, the necessary resistance is:

$$R = 1/(2\pi \times (2 \times 10^{-6}) \times 6Hz)$$
$$R = 13.263k$$

The resulting response times with these R and C values would be:

$$t(1\%) = 4.6RC = 122ms$$
$$t(0.1\%) = 6.9RC = 183ms$$
$$t(0.01\%) = 9.2RC = 244ms$$

Note that there are a number of RC values that can be used in a given situation. To minimize the effects of the series resistance, however, it s recommended that the value of R be kept under 20kΩ.

Current-to-Voltage Conversion

AMM1A local inputs are designed to accept voltages in the range of ±10V. Thus, the AMM1A can be directly connected to many signal sources. Some transducers and instrumentation, however, provide current outputs that must be converted into voltages in order to be measured through an AMM1A input channel.

When connecting current inputs to the AMM1A, a resistor should be installed across the input to make the necessary current-to-voltage conversion. J4, J5, and J6 provide locations for installing these resistors on the AMM1A. Refer to the circuit schematic and board layout diagrams for header information.

The value of the resistor can be determined from Ohm's Law as follows:

$$R = E/I$$

Where R is the resistance in ohms, E is the maximum desired voltage in volts (usually the upper range limit of the A/D converter), and I is the maximum anticipated current in amps.

As an example, assume the A/D converter range is zero to +10V and that the expected current lies in the range of four to 40mA. The required resistance is:

$$R = 10/0.04$$
$$R = 250$$

Thus, a 250Ω resistor should be installed across the input of the channel in question (note that a 250Ω value is required when using KDAC500 engineering units conversion). Since current measurement accuracy is directly related to the accuracy of the resistor, use the smallest tolerance resistor available (typically 0.1%). Suitable 250Ω precision resistors can be purchased from Dale Resistors, (P/N RN55E2500B), or from Keithley (P/N 500-RES-250).

Analog-to-Digital Converter Timing

When programming high-speed sampling sequences, certain timing constraints concerning the A/D conversion cycle should be observed. Depending on the AMM1A's acquire mode, the scenario for receiving converted values from the A/D is very different. Refer to the discussion of the acquire modes below for specific instruction on how to process analog signals.

To increase system throughput, data latches have been provided on the AMM1A, making data from the last conversion available while the converter is busy processing another reading. The data is refreshed (updated) every time a conversion has been completed.

External Trigger Operation.

The AMM1A has the capability of triggering an acquisition from an external TTL-level source. The jumper on the AMM1A (J3) dictates the triggering source. The external trigger can only be used in 62.5kHz auto acquire mode which is explained below in the SET ACQUISITION MODE command discussion.

When the AMM1A is in 62.5kHz auto acquire mode, the trigger source can be set to either external or internal by the J3 jumper. When set for internal triggering, the AMM1A continuously converts analog signals as described below in the SET ACQUISITION MODE command discussion. When the J3 jumper is removed, a TTL-level gating signal can be attached to pin 2 of the jumper header. A low level applied to pin 2 will enable the continuous conversion process, a high level applied to pin 2 will suspend the

continuous conversion process. In either case, the application program must synchronize itself to the conversion process by polling the conversion status as explained in the SELECT ACQUISITION MODE command discussion.

The pin configuration of the jumper header is as follows:

pin 1 Special trigger output - valid only when using TRG1
pin 2 trigger input
pin 3 0V (ground) - for internal triggering

The J3 jumper should be across pins 2 and 3 for internal trigger operation. The jumper should be removed and the external gating source should be connected to pin 2 for external gate operation. The J3 jumper should be across pins 1 and 2 if a TRG1 analog trigger module is being utilized.

Commands

Table 1 summarizes the commands used with the AMM1A. Note that several commands share the CMDA and CMDB locations. Some commands use only selected bits in the command byte, others are differentiated by whether a read or write operation is performed.

Table 1. Commands Used with the AMM1A

Command	500/575 Address	Signal Line	Bits Used
SELECT CHANNEL	xxx80	CMDA (Write)	D0-D3
SELECT LOCAL CHANNEL MODE	xxx80	CMDA (Write)	D4
SELECT LOCAL GAIN	xxx80	CMDA (Write)	D5
SELECT ACQUISITION MODE	xxx80	CMDA (Write)	D6
SELECT FILTER	xxx80	CMDA (Write)	D7
SELECT SLOT	xxx81	CMDB (Write)	D0-D3
SELECT CMDA READ MODE	xxx81	CMDB (Write)	D4
SELECT RANGE	xxx81	CMDB (Write)	D5
SELECT GLOBAL GAIN	xxx81	CMDB (Write)	D6-D7
RESET AND RECAL	xxx9A	CMDC (Write)	ALL
A/D LOW DATA*	xxx80	CMDA (Read)	ALL
A/D STATUS*	xxx80	CMDA (Read)	ALL
A/D HIGH DATA	xxx81	CMDB (Read)	ALL
A/D START	xxx9B	CMDD (Write)	ALL
EOC (end-of-conversion) STATUS	xxx9B	CMDD (Read)	ALL

*The information read from CMDA is selected by the SELECT CMDA READ MODE command. Refer to the sections below for the full description of their operations.

The "xxx" in the 500/575 address column signifies the three hexadecimal digits that make up the base hardware address which is either switch selected or programmed on the IBIN-A or IBIN-PS/2 interface card. The suggested address is &HCFF80, so "xxx" = "&HCFF".

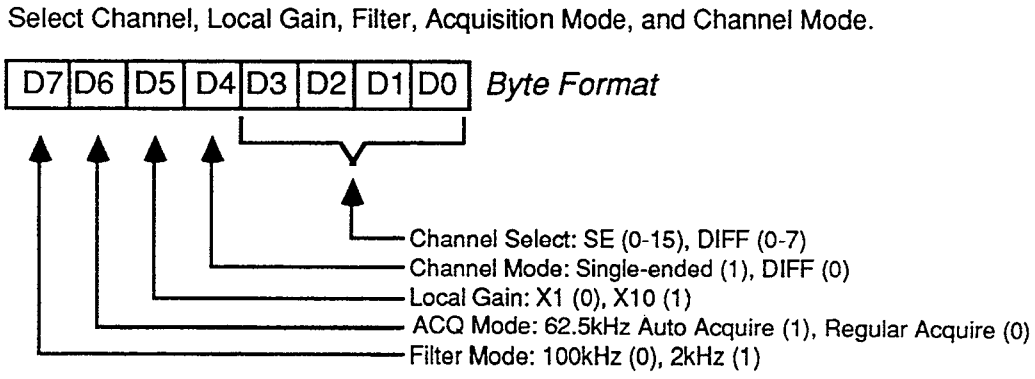


Figure 5. CMDA Write Format

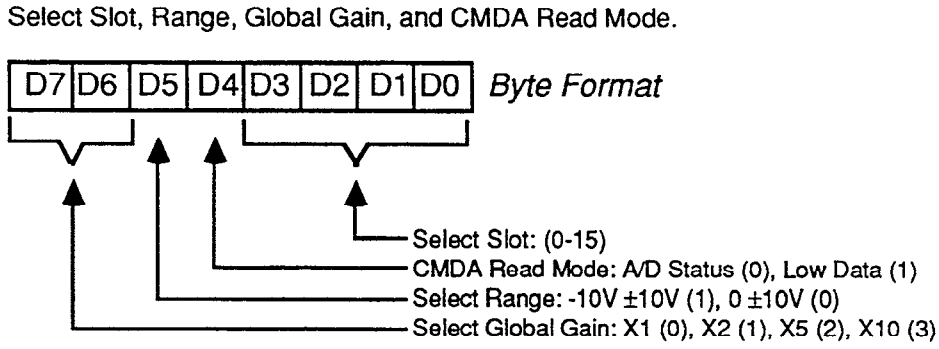


Figure 6. CMDB Write Format

SELECT CHANNEL

Location: xxx80

The SELECT CHANNEL command is used to control the local signal multiplexer on the AMM1A, thus determining which of the local input channels is selected for A/D conversion. This command affects only those signals connected to the AMM1A local inputs, and does not affect input channels connected to modules located in other slots. SELECT CHANNEL must be used in conjunction with the SELECT SLOT command to select the channels on the AMM1A to be measured.

Note that the channel number occupies the least significant four bits of CMDA. Make sure that the channel number is combined with the appropriate upper four bits, as shown in Figure 5, before it is sent.

SELECT LOCAL CHANNEL MODE

Location: xxx80

The SELECT LOCAL CHANNEL MODE command controls the configuration of the local input channels on the AMM1A. The AMM1A input channels can be configured as either 16 single-ended or eight differential input channels. This command is selected by assigning a value to the D4 position of CMDA as shown in Figure 5. A value of 1 will set the inputs to single-ended, a value of 0 will set them to differential.

Make sure that the other bits in the CMDA byte represent the desired selections before it is sent.

SELECT LOCAL GAIN

Location: xxx80

The gain applied to the local channels of the AMM1A is programmable and can be set by assigning a value to bit position D5 in CMDA. As shown in Figure 5, a value of 0 will apply a local gain of X1 and a value of 1 will apply a local gain of X10 to the AMM1A input channels.

The local gain can be changed at any time as long as the channel settling time is satisfied before the conversion is started.

Make sure that the other bits in the CMDA byte represent the desired selections before it is sent.

SELECT ACQUISITION MODE

Location: xxx80

The AMM1A has the capability of operating in either of two modes; the regular acquisition mode, and the 62.5kHz auto acquisition mode. As shown in Figure 5, the acquisition mode is set by assigning a value to bit position D6 in CMDA. Assigning a value of 0 enables regular acquisition mode, a value of 1 enables 62.5kHz auto acquisition mode.

To acquire an analog reading when in the regular acquisition mode, the slot, channel, and gain must be selected. Then, after the appropriate settling time, the AMM1A is issued a START CONVERSION command. At this time, the AMM1A latches the signal and starts the digitization process. The EOC STATUS command can be polled for end-of-conversion (EOC) after which the digitized value can be read. The conversion process will consume approximately 16µsec.

Since the incoming signal is latched when the START CONVERSION command is issued, the slot, channel, and gain selections can be changed immediately after the command is issued. This will allow the settling time for the new selections to be satisfied concurrently with the conversion of the previous selection. This type of operation is not required but will increase the throughput capability of regular acquisition mode.

The auto acquisition mode allows full 62.5kHz acquisition speed on analog signals. Upon placing the AMM1A in this mode, the A/D enters a free-running 62.5kHz conversion process. Do not attempt to issue the START CONVERSION command in this mode.

Some microcomputers may not be capable of keeping up with the AMM1A in auto acquire mode. If the AMM1A outpaces your microcomputer, the data points will be unreliable.

After the completion of a conversion, the AMM1A begins the next conversion immediately. The EOC STATUS command can be used to synchronize your program with the conversions. The conversions will take place on the slot and channel that are presently selected at a rate of 62.5kHz. The conversion status bit will be reset by the reading of either the high or low A/D data bytes. Figure 7 shows the timing for single channel auto acquire operation.

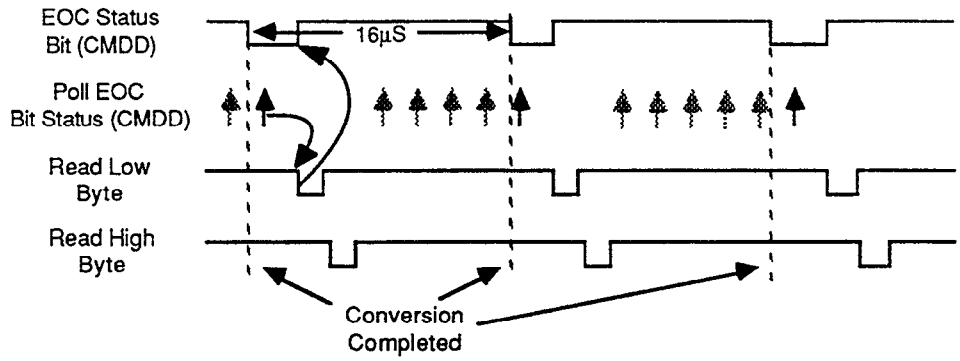


Figure 7. Single Channel Auto Acquire Timing

While in auto acquire mode, the EOC status bit will become true (low) after the first A/D conversion. Even though the next conversion begins immediately, the status bit remains true until the A/D data is read. If the data is not read, it is overwritten.

Figure 8 shows a example of the EOC status being polled only after one or more conversions have taken place. Even though the EOC status bit indicates that the conversion is complete, there is no way of telling if another conversion is about to be completed. Trying to read the data while the latches are being updated will cause unreliable results. To guarantee reliable readings, your program should synchronize itself with the AMM1A by taking a dummy reading to clear the conversion status bit. The next time the status bit indicates the end of a conversion, the data at the A/D latch will be valid for the full 16µsec.

For multichannel auto acquisition operation, all of the settling times for the new channel must be satisfied 4µsec before the EOC takes place. If it is not settled, it may be necessary to throw away a reading or two until it has settled. To maximize the available settling time, it is recommended that slot selection, gain selection, and channel selection take place directly after the EOC becomes true.

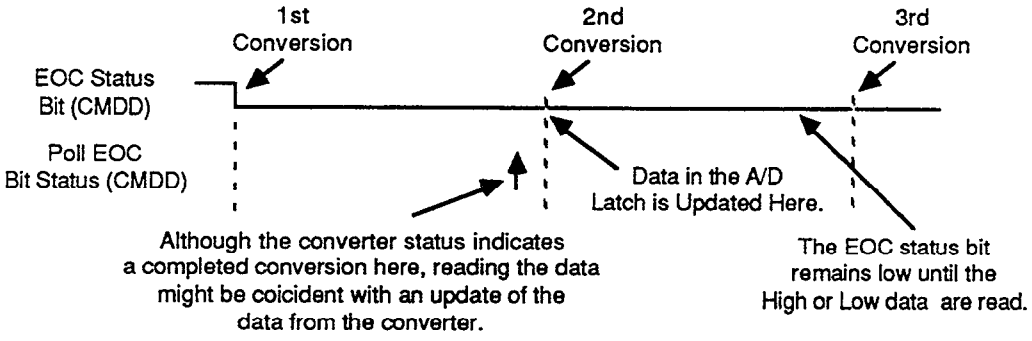


Figure 8. Polling the Status Bit After One or More Conversions

For optimum operation follow these steps:

1. Monitor the EOC status bit until an end-of-conversion is sensed.
2. Select a new gain, a new slot, and a new channel, as needed.
3. Read the latched data from the last conversion.

A timing diagram for multichannel operation is shown in Figure 9.

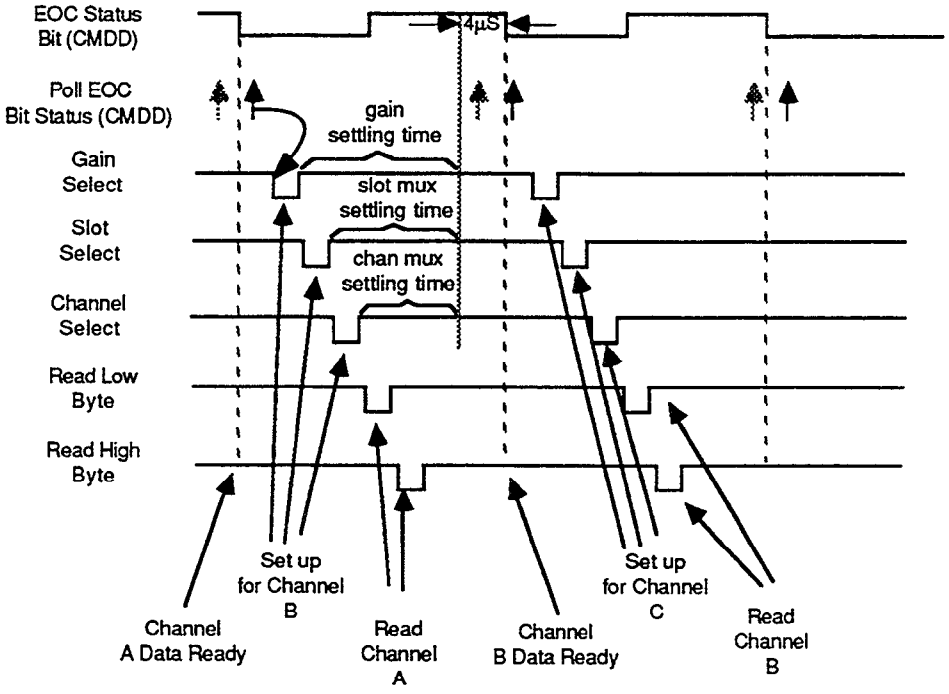


Figure 9. Multichannel Operation in Auto Acquire Mode

Even though the AMM1A is capable of digitizing analog signals at 62.5kHz, some modules in the Series 500 module library are not capable of settling at these speeds. When doing multichannel acquisition, consult the individual module's hardware manual for appropriate settling times.

SELECT FILTER

Location: xxx80

Two filters are available in the AMM1A; a 100kHz filter, and a 2kHz filter. These filters restrict the bandwidth of the incoming signal, rejecting either noise or unwanted high frequency components that may create aliasing.

It is desirable to reject all signal frequency components that are greater than 1/2 the sampling frequency. These frequency components cause aliasing which produces inaccurate waveform representation. The filters are designed to reject frequencies above 100kHz or above 2kHz, depending on the filter used. The 100kHz filter, while not providing complete protection against aliasing, does reduce the system noise with a minimal effect on settling time.

Assign a value of 0 to bit position D7 in CMDA to select the 100kHz filter, assign a value of 1 to select the 2kHz filter.

Make sure that the other bits in the CMDA byte represent the desired selection before it is sent.

SELECT SLOT

Location: xxx81

The SELECT SLOT command controls the global multiplexer on the AMM1A, selecting the appropriate slot on the Series 500 baseboard from which to read the input.

The value to be written to the SELECT SLOT location occupies the four least significant binary digits of the command. Make sure that the slot number is combined with the appropriate upper four bits as shown in Figure 6 before it is sent.

As indicated in Table 2, there are other values besides slot numbers that can be written to this location. These values select ground, +5V, and +10V sources and are intended primarily for diagnostic purposes.

Table 2. Values Written to the SELECT SLOT Location

Function	Binary
Ground (0 volts)	bbbb0000
Slot 1	bbbb0001
Slot 2	bbbb0010
Slot 3	bbbb0011
Slot 4	bbbb0100
Slot 5	bbbb0101
Slot 6	bbbb0110
Slot 7	bbbb0111
Slot 8	bbbb1000
Slot 9	bbbb1001
Slot 10	bbbb1010
Reserved	bbbb1011
Reserved	bbbb1100
+10V Reference	bbbb1101
Ground (0 volts)	bbbb1110
+5V Digital Power Supply	bbbb1111

SELECT CMDA READ MODE

Location: xxx81

This command selects the usage of the CMDA read. Two types of information can be read from CMDA (note that this affects only the read operation of CMDA), these are, the low data byte of the A/D or the A/D status. In the low data byte mode, CMDA supplies the low byte of the A/D readings. In the A/D status mode, CMDA supplies status directly from the A/D. The A/D status is described further in the sections below.

NOTE: When the CMDA read mode is set to A/D status, a reset and recal sequence will be initiated by any start conversion command. The start conversion command can come either from a write to CMDD, or from the auto acquire mode hardware if this mode has been enabled by a value of 1 in bit position D6 of CMDA. To avoid accidentally initiating a reset and recal sequence, be sure bit position D6 of CMDA is set to a value of 0 before changing the CMDA read mode to A/D status. Do not write to CMDD or change D6 of CMDA to a value of 1 as long as the CMDA read mode is set to A/D status.

Assign a value of 0 to bit position D4 in CMDB to read A/D status from CMDA, assign it a value of 1 to read the A/D low data byte.

Make sure that the bit is combined with the other appropriate bits as shown in Figure 6 before it is sent.

SELECT RANGE

Location: xxx81

The AMM1A has two programmable ranges; ±10V (bipolar 10V) and zero to +10V (unipolar 10V). Assigning a value of 0 to bit position D5 in CMDB will select the AMM1A unipolar 10V range, assigning a value of 1 will select the bipolar 10V range.

Make sure that this bit is combined with the other appropriate bits as shown in Figure 6 before it is sent.

SELECT GLOBAL GAIN

Location: xxx81

The GLOBAL GAIN command controls the PGA (Programmable Gain Amplifier) located on the AMM1A module. Since all analog inputs are processed by the PGA, the GLOBAL GAIN command affects every analog input connected to the Series 500. This command is issued in combination with other commands on CMDB. The GLOBAL GAIN value occupies the two most significant bits of CMDB and must be combined with the other bits of the CMDB byte before it is issued.

Four programmable gain values, x1, x2, x5, and x10, are available with the PGA. These gains are selected by setting the appropriate bits in CMDB before it is issued.

Table 3. Values Written to the GLOBAL GAIN Location

PGA Gain	Binary
x1	00bbbbbb
x2	01bbbbbb
x5	10bbbbbb
x10	11bbbbbb

RESET AND RECAL

Location: xxx9A

The RESET AND RECAL command starts the internal A/D calibration process. The process takes approximately 360msec and should be completed once every time the system is powered up.

After issuing this command, wait at least 360msec before any conversions are attempted. To make sure that the calibration has taken place, set the CMDA read-mode to A/D status, as described above. The bit configuration of the calibration status is described below. This bit can be polled to make sure calibration has been completed.

This command has no specific data associated with it, any value sent will start the calibration process.

A/D LOW DATA - A/D STATUS

Location: xxx80

The contents of CMDA depends on the state of the AMM1A set by the SELECT CMDA READ MODE command. If D4 of CMDB has been set to 0, CMDA returns the A/D status of the AMM1A. If D4 has been set to 1, the low byte of the A/D counts is returned in CMDA.

When AMM1A is in the A/D status mode, the bit configuration of the CMDA byte is as follows:

D0 none
D1 none
D2 none
D3 none
D4 none
D5 TRACKING (1=tracking in process, 0=tracking stopped)
D6 CONVERTING (1=conversion in process, 0=no conversion in process)
D7 CALIBRATING (1=calibration in process, 0=calibration not in process)

After the A/D completes a digitization of an analog signal, it begins a process called tracking. The A/D consumes 4µsec for the analog signal at its input to be tracked to the specified accuracy. The time relationship between the TRACKING bit and the EOC bit in CMDD is shown in Figure 10.

The converting bit indicates the actual A/D conversion status. The time relationship between the CONVERTING bit and the EOC bit in CMDD is shown in Figure 10.

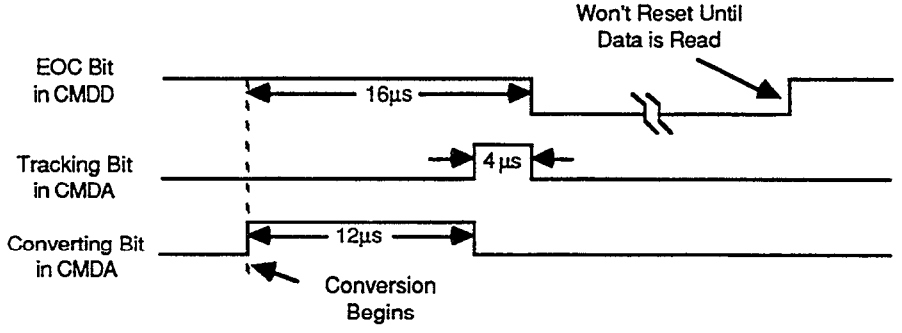


Figure 10. Time Relationship of Status Bits

The CALIBRATING bit returns the status of a RESET AND RECAL command as described above.

If the AMM1A is in the low data mode, the byte received is the low byte of a 16 bit A/D conversion. However, the 4 least significant bits will be set to 0, thereby providing 12-bit resolution effectively. Since the module incorporates data latches, one conversion may be read while another conversion is in

progress. To find out when data from one conversion is available, use the A/D START/EOC STATUS command, discussed below.

Reading this location resets the EOC status.

A/D HIGH DATA

Location: xxx81

The A/D HIGH DATA command performs essentially the same function as the A/D LOW DATA command, except that the high data byte is returned. Since the AMM1A's 12-bit resolution is actually the result of setting the four least significant bits of a 16-bit conversion to 0, all of the bits in the high data byte of an AMM1A are significant.

Once both the low and the high data bytes have been obtained, the total number of counts representing A/D converter data can be determined using the following formula:

$$CO = DL + 256*DH$$

CO represents the number of counts, and DL and DH are the low and high bytes respectively. With the AMM1A, the number of counts will lie in the range of 0 to 65,535 minus 4 least significant bit's worth, or 0 to 65520.

Reading this location resets the EOC status.

A/D START

Location: xxx9B

The A/D START COMMAND starts the A/D conversion process. Writing to the A/D START location will trigger (start) the A/D conversion cycle. Although any value (0-255) can be written to trigger a conversion, a value of 255 should be used to minimize noise. Do not issue an A/D start command while in auto acquisition mode or the internal timing of the A/D will be skewed.

The A/D conversion cycle takes approximately 16µsec. During this period, the converter should not be re-triggered. Status of the conversion process can be checked by accessing the EOC STATUS command.

EOC STATUS

Location: xxx9B

The EOC STATUS command returns a byte of data which indicates the state of the conversion process. The returned value will depend on whether a conversion has been completed (see Table 4).

Table 4. Values Read from the A/D START/STATUS Location

EOC Status	Binary
Conversion in process	1xxxxxxx
End-of-conversion	0xxxxxxx

Calibration

This section contains calibration procedures for the AMM1A module. The procedures include programs which have been written with BASIC's PEEK and POKE commands for use on a Series 500 or 575. Note that these procedures are intended for the field and may not be as accurate as those used in the factory. If you are not familiar with calibration equipment, do not attempt AMM1A calibration.

This procedure presumes that the unit is in working condition and at least one factory calibration has been done in the past. An additional procedure is necessary to select R25, R26, R27 and R28 if the voltage reference U13 has been replaced. The procedure for replacing U13 is described after the section on troubleshooting.

Environmental Conditions

Calibration should be performed at an ambient temperature of 23°C (±5°). Turn on the system power and allow it to warm up for at least 10 minutes before beginning the calibration procedure.

Recommended Calibration Equipment

The following equipment is recommended for AMM1A calibration. Other equipment may be used as long as the corresponding specifications are at least as good as those given below.

1. Keithley Model 196 DMM (0.005% basic DC accuracy).
   Key specs needed on DMM:
   DC accuracy of 60 ppm on a 10V reading.
   Sufficient resolution to read one microvolt offsets.

2. EDC Model E100C Millivolt Reference Source (0.005% accuracy).
   Key specs needed on source:
   Provides an output between 0.5 and 0.99 volts.
   Maintains its output stable to 10 ppm for five minutes.

Overview of Adjustment Sequence

1. Adjust 10V reference.
2. Adjust 4V reference.
3. Adjust Global Amp offset.
4. Adjust attenuator offset.
5. Adjust both Local amp offsets.
6. Adjust Local amp X10 gain.
7. Tweak A/D gain with 4V reference adjustment.

Calibration Procedure

The test points, potentiometers, and connectors referenced in the procedure are shown in Figure 1.

Adjust 10V reference

1. Connect the DMM high lead to TP7 (10V). Connect the DMM low lead to TP4 (AGND). Select DCV and autoranging.
2. Adjust pot R7 for 10.0000 volts ±100µV.

Adjust 4V reference

The following procedure will bring the 4V reference within range so that it can be calibrated accurately later.

1. Connect the DMM high lead to TP8 (4V). Connect the DMM low lead to TP4 (AGND). Select DCV and autoranging.
2. Adjust pot R8 for 4.000 volts ±1mV. This adjustment will be tweaked later.

Adjust Global Amp offset

1. Connect the DMM high lead to TP9. Connect the DMM low lead to TP4 (AGND). Select DCV and autoranging.
2. Select the PGA gain of X10 and the zero voltage reference input by POKEing a value of 192 to CMDB of slot 1 and a value of 0 to CMDA of slot 1.
3. Adjust pot R9 for zero volts ±10µV.

Adjust attenuator offset

1. Select the X1 global gain and the zero voltage reference input by POKEing a value of zero to both CMBA and CMDB of slot 1.
2. Connect the DMM high lead to TP10. Connect the DMM low level to TP9. Select DCV autoranging.
3. Adjust pot R10 for zero volts ±10µV.

Adjust both Local amp offsets

1. Connect a short jumper wire between differential channel 0 high input and signal common (terminals 9 and 10 on J1). Connect a short jumper wire between differential channel 0 low input and signal common (terminals 1 and 2 on J2).
2. Connect the DMM high lead to TP3. Connect the DMM low lead to TP4. Select DCV and autoranging.
3. Select differential input and X1 gain by POKEing a value of 0 to CMDA of slot 1.
4. Record the DMM reading as Vout(1) for use later.
5. Select a gain of X10 by POKEing a value of 32 to CMDA of slot 1.
6. Record the DMM reading as Vout(2).
7. Compute the offset contribution of U6 as follows: $V_{OS} = (10*V_{OUT}(1) - V_{OUT}(2))/9$.
8. Adjust pot R5 so that the DMM reads the voltage computed for V_{OS}.

9. Select the X1 gain again by POKEing a value of zero to CMDA of slot 1.
10. Adjust pot R6 for a DMM reading of zero volts ±10μV. If desired, the adjustment can be checked by once again outputting data: CMDA = 32. The DMM should read zero volts ±100μV.

Adjust Local amp X10 gain

1. Remove the jumper between terminals 9 and 10 of J1 that was installed in previous step. Connect voltage source (+) output to terminal 9 of J1, and the voltage source (-) output to terminal 10 of J1. Leave the jumper installed between terminals 1 and 2 of J2.
2. Connect the high lead of the DMM to TP3. Connect the low lead of the DMM to TP4. Select DCV and autoranging.
3. Set the voltage source to a value of 0.99 volts.
4. Select the X10 gain by POKEing a value of 32 to CMDA of slot 1.
5. Adjust pot R4 for a reading of 9.9 volts.

Tweak A/D gain with 4V reference adjustment

1. Use the test setup from the previous step. The DMM should be reading a voltage of approximately 9.9 volts on TP3.
2. Select channel 0, local gain of X10, differential input, filter on (2kHz), slot 1, unipolar 10V range, and global gain of X1 by POKEing values of 160 and 17 to CMDA and CMDB respectively.
3. Run the following BASIC program. This program assumes that the hardware address in CFF0, if this is not the case, adjust line 10 for the proper address.

```
 10  DEF SEG = &hCFF0                    'hardware segment*
 20  CMDA = &h80: CMDB = &h81
 30  CMDC = &h9A: CMDD = &h9B
 40  POKE CMDA, 160                      'set up from step 2 above
 50  POKE CMDB, 17                       'set up from step 2 above
 60  POKE CMDD, 255                      'start conversion
 70  WHILE PEEK(CMDD) > 127 :WEND        'wait until conversion is complete
 80  TOTAL = PEEK(CMDA) + PEEK           'get high and low data and combine
     (CMDB)*256
 90  VOLTS = TOTAL * 0.00015258
100  LOCATION 1,1:PRINT VOLTS,           'print value in volts
110  GOTO 60
```

*Presumes interface is set to address CFF80(h).

4. Adjust pot R8 so that the displayed voltage equals the DMM reading.

Theory of Operation

For the following discussion, please refer to the schematic diagram, drawing number 501-196.

AMM1A circuitry is divided into the following sections: local input multiplexer, programmable gain, global input multiplexer, global gain amplifier, filter, A/D converter, A/D voltage reference amplifier, and the 10-volt global reference.

Local Input Multiplexer

The local input multiplexer is made up of two 8 to 1 analog multiplexer U1 and U2, a dual analog switch U3, and input protection resistor networks R1 and R2. The digital control signals for the input multiplexer are latched by U19, and additional digital logic to control the differential/single-ended mode selection is in the PAL, U18. When the single-ended mode is programmed, U3 grounds the inverting input of the differential instrumentation amplifier (pin 3 of U7), and connects the output of both U1 and U2 to the non-inverting input of the differential instrumentation amplifier (pin 3 of U5). The selected input is switched through the appropriate 8 to 1 multiplexer to the differential amplifier input while the output of the other 8 to 1 multiplexer is open circuited. When the differential input mode is selected, U3 connects the output of U2 to the inverting input of the differential instrumentation amplifier (pin 3 of U7). The output of U1 is always connected to the non-inverting input of the differential instrumentation amplifier (pin 3 of U5). The selected input channel -CH terminal is connected through U2 and the +CH terminals is connected through U1 to the local amplifier inputs.

Local Programmable Gain Amplifier

U4, U5, U6 and U7 make up the local programmable gain amplifier. U5 and U7 provide the high input impedance, and also provide the voltage gain when the X10 gain is selected. When X1 gain is selected, U4 (a dual analog switch) connects both U5 and U7 in the voltage follower configuration. When X10 gain is selected, U4 connects the inverting inputs of U5 and U7 to the taps on a voltage divider connected across the outputs of U5 and U7. The voltage difference between the inverting inputs of U5 and U7 is 1/10 the voltage difference between the outputs of U5 and U7. This arrangement gives a voltage gain of 10 for differential input signals and a voltage gain of 1 for common mode input signals. The common mode input signal is defined as the average of the +CH and -CH input signals. The voltage gain in the X10 mode is adjusted with R4, which adjusts the voltage divider ratio. The voltage gain in the X1 mode is not adjustable. The outputs of U5 and U7 are connected to the precision resistor network R11 and amplifier U6. R11 and U6 make up a unity gain differential amplifier, which amplifies the differential signal and rejects the common mode signal. The output of U6 is the overall amplifier output, and consists only of the differential signal between U5 pin 3 and U7 pin 3.

Global Input Multiplexer

The global multiplexer selects which signal is measured by the A/D converter. U8 is a 16 to 1 analog signal multiplexer. Inputs 0 and 14 of U8 are connected to ground. Input 1 is connected to the output of the local amplifier. Inputs 2 through 10 go to pins on P14, and by external connections, are connected to slots 2 through 10 of a Series 500 mainframe. These connections will carry the output signals of other signal processing cards to the global multiplexer, where they can be routed to the A/D converter for measurement. Inputs 11 and 12 also go to J14, but are typically not used. Input 13 is connected to the 10-volt reference, and input 15 is connected to the +5-volt digital power supply. The output of the multiplexer is connected to the Global Amplifier input.

Global Programmable Gain Amplifier and Filter

The global programmable gain amplifier is made up of U9, U10, and U11. The voltage gain of U9 is determined by which tap on the precision resistor network R14 is selected by the analog multiplexer U11. The available gains are X1, X2, X5, and X10. R14 is a voltage divider connected to the output of U9, and the tap determined by U11 is connected to the inverting input of U9. The non-inverting input of U9 is the overall input of the circuit. At the output of U9, 10 volts represents a full scale input. The A/D converter used cannot convert an input above 4 volts, so that output of U9 is reduced to 40% of its full scale output by a divider made up of R15, R16, and R17. The analog filter is applied after this divider, and is made up of C7 and R18 along with the combined resistance of the divider. For the 2kHz pole, all resistors are in the circuit, but when the 100kHz pole is programmed, FET Q3 is turned on and bypasses R18. The 100kHz pole is determined by the equivalent output resistance of the 40% divider and C7. U10 buffers the filter output and provides the low driver impedance required by the A/D converter. At the output of U10, 4 volts represents a full scale input. CR1, CR2, CR3, and CR4 make up a clipping circuit to prevent overscale inputs from saturating the A/D, thus allowing immediate overload recovery.

A/D Converter

The A/D converter, U12, is a 12-bit successive approximation converter with an internal sample and hold. This converter is similar to the A/D converter on the 16-bit AMM2 module in that both converters read as 16-bit converters. Like the AMM2, the AMM1A returns a high and low byte. However, the four lowest order bits from the AMM1A are zeros, thus providing 12 effective bits of resolution. U12 operates on +5 volts and -5 volts. These supplies are derived from the +15 and -15 volt analog supplies by U21 and U22 respectively. The A/D determines the ratio of the analog input to the voltage reference input. The voltage reference used is 4 volts. The digital outputs of the A/D reference input. The voltage reference used is 4 volts. The digital outputs of the A/D are buffered by U16 and U17. The logic control for the A/D is in the PAL, U18.

A/D Voltage Reference Amplifier

The A/D converter requires a voltage reference source with a low output impedance from dc up to several megahertz. U15, Q1, R8 and the associated components comprise an amplifier with the needed characteristics. The reference voltage is derived from the heated zener reference U13 and divided down to 4 volts by the divider made up of R8, R21, R22, and R24. Resistors R27 and R28 are used to restrict the adjustment range of R8, and are either installed or not used based upon the zener voltage of Y13 at the time of factory calibration. If U13 is replaced, it may be necessary to either install or remove either one or both of these resistors. R31 and C6 frequency compensate the amplifier loop, and C9 is a filter for zener noise.

10 Volt Global Reference

U13, U14 and the associated components form the 10 volt reference circuit. The zener voltage of approximately 7 volts is amplified by U14 to 10 volts. R7, R19, R20, and R23 determine the output voltage by adjusting the gain of U14. R25 and R26 serve a function similar to R27 and R28 in the A/D reference circuit. R30 and C8 filter the zener noise, and D7 assures that the circuit will start properly when power is first applied.

AMM1A Troubleshooting Information

Diagnosing trouble with the AMM1A is best done in several steps. If the AMM1A is not functioning at all, the following tests should be performed in the sequence indicated. It may be possible to skip some of the tests if the AMM1A is partially functional.

A BASICA test program is listed at the end of this section which is used to setup the hardware for these tests. Change line 10, if necessary, to the address segment used by your system. Each test is independent, and can be run by itself if needed, as long as the first 3 lines of the program are also entered.

The overall test sequence is:

1. Check power supplies
2. Check reference voltages
3. Test digital control circuitry
4. Test local mux
5. Verify operation of local amplifier
6. Check operation of global amp
7. Test global mux
8. Verify operation of A/D converter

The only additional equipment needed for these tests is a digital multimeter (DMM), and two jumper leads. When performing these tests, refer to schematic diagram 501-196, component layout 501-190, and the following instructions for the connections to use while running the test program.

Test Sequence:

1. Check power supplies

   Using a DMM on the 20-volt range, connect the minus lead to TP4 (AGND). The positive lead should be used to test for the following voltages within ±0.5 volts:

U7 pin 7	+15
U7 pin 4	-15
TP6 (DIG GND)	0
U18 pin 24	+5
U12 pin 25	+5
U12 pin 11	+5
U12 pin 30	-5
U12 pin 36	-5

2. Check reference voltages

   With the DMM minus lead connected to TP4 (AGND), use the 20-volt range to read the following voltages:

TP14 (Vz)	7 ±0.25 volts	zener reference voltage

TP7 (10Vref)	10.00 volts	U14 output
TP8 (4V)	4.0 ±0.2 volts	U15 output, A/D reference voltage

3. Test digital control circuitry

   Use the test program lines 300-395 to verify that the control registers are capturing the correct data. Connect the minus lead of the DMM to TP6 (DGND) and touch the DMM plus lead to the pins indicated by the program.

   If this test is completely unsuccessful, first verify that the rest of the system is functioning properly before proceeding. The computer, IBIN interface card, 500 mainframe, and hardware address segment should be checked. If the rest of the system is functioning properly, or if only some of the pins on U19 or U20 are not functional, check U18, U19, U20 and the IC's connected to the nonfunctional pins.

4. Test local mux

   The local mux can be checked by putting a signal through each of its channels. A convenient signal is the 4-volt reference tested in step 2. The test program lines 400-490 will help perform the test. Connect a test lead to TP8 (4V) and connect the other end of this test lead to the input on J1 or J2 as indicated by the program. Connect the DMM - lead to TP4 (AGND), and the + lead to TP1 or TP2 as indicated by the program. Run the program. The DMM should show the 4-volt signal on the indicated test point when the input indicated by the program is touched with the 4V test signal.

5. Verify operation of local amplifier

   Proper operation of the local amplifier can be tested by applying a voltage difference of one volt to its input and looking for an output of one volt on the X1 gain range and 10 volts on the X10 gain range. A one volt signal can be obtained by connecting +4V reference TP8 (4V) to -CH0 on J2 pin 2, and +5V supply TP12 (+5V) to +CH0 on J1 pin 9. Connect the DMM + lead to TP3 and the - lead to TP5 (SGND). Lines 500-580 provide the setup for this test.

6. Check operation of global amp

   The global amp can be tested by using the one volt signal generated in step 5 above, and checking that the correct output at TP9 occurs for each gain setting. The global mux channel 1 of U8 must be functional for this test to work, so it is checked first. Connect a test lead from TP8 (4V) to J2 pin 2 and a second test lead from TP12 (+5V) to J1 pin 9. The DMM - lead connects to TP4 (AGND), and the + lead to the TP indicated as the output in the test program. Lines 600-690 of the test program are used.

7. Test global mux

   The global mux is tested by applying a signal to each input and verifying that the signal appears at the output. Since the global amp was tested in the previous step, any signal applied to the global mux should show up at TP9. The slot inputs can be tested by applying the 4-volt reference signal to the input under test. Other inputs to the global mux are hardwired to various signals as indicated by the program. Setup the test as follows: Connect a test lead from TP8 (4V) to J2 pin 2 and a second test lead from TP12 (+5V) to J1 pin 9. The DMM - lead connects to TP4 (AGND), and the + lead to TP9. At the point in the program where a signal is required as an input to a pin on U8, disconnect the end of the test lead on J2 pin 2 and use this end to touch the pin indicated by the program on U8. Lines 700-790 of the test program are used.

8. Verify operation of A/D converter

The A/D converter is tested by inputting a signal from the local amp and displaying the reading. The test setup uses the one volt test signal derived in step 5. The displayed voltage should be about one volt. Connect a test lead from TP8 (4V) to J2 pin 2 and a second test lead from TP12 (+5V) to J1 pin 9. Lines 800-890 of the test program are used.

Replacement Procedure for U13

The heated zener voltage reference U13 requires a special calibration procedure if it is replaced. The LM399 used for U13 has a wide tolerance for its initial zener voltage, but drifts very little with time or temperature. Resistors R25, R26, R27 and R28 are used to trim out a large portion of the initial zener voltage tolerance, with the balance of the adjustment done by potentiometers R7 and R8. The adjustment range of R7 and R8 is large enough to compensate for any drift in U13 over the life of the module, but has been purposely restricted to improve the stability and adjustability of the voltage reference. When U13 is replaced, the following procedure must be used to determine which two of the four resistors (R25, 26, 27,28) must be installed.

The procedure is to measure the zener voltage, + lead to TP14, - lead to TP4 (AGND), find the range on the following table that includes this voltage, then install or remove the resistors indicated in the table as required.

Zener Voltage	R25	R26	R27	R28
6.78 to 6.90	open	61.9 K	383 K	open
6.90 to 7.01	49.9 K	61.9 K	open	open
7.01 to 7.11	open	open	383 K	267 K
7.11 to 7.23	49.9 K	open	open	267 K

Troubleshooting Test Program

```
 10   DEF SEG = &HCFF0                          'HARDWARE SEGMENT
 20   CMDA = &H80:  CMDB= &H81
 30   CMDC = &H9A:  CMDD = &H9B
300   CLS
310   PRINT "3. TEST DIGITAL CONTROL CIRCUITRY"
320   POKE CMDA, 255
330   PRINT "MEASURE > 3 VOLTS ON PINS 2, 5, 6, 9, 12, 15, 19 OF U19"
335   INPUT "PRESS RETURN TO CONTINUE", A$
```

```
340   POKE CMDA,0
350   PRINT "MEASURE < 1 VOLT ON PINS 2, 5, 6, 9, 12, 15, 19 OF U19"
355   INPUT "PRESS RETURN TO CONTINUE", A$
360   POKE CMDB,255
370   PRINT "MEASURE > 3 VOLTS ON PINS 2, 5, 6, 9, 12, 15, 19 OF U20"
375   INPUT "PRESS RETURN TO CONTINUE", A$
380   POKE CMDB,0
390   PRINT "MEASURE < 1 VOLT ON PINS 2, 5, 6, 9, 12, 15, 19 OF U20"
395   INPUT "PRESS RETURN TO CONTINUE", A$
400   CLS
405   PRINT "4a. TEST LOCAL MUX SINGLE ENDED MODE"
410   FOR N = 0 TO 15
415   IF N < 8 THEN PIN = 9 - N ELSE PIN = N - 6
420   IF N < 8 THEN J = 1 ELSE J = 2
425   POKE CMDA, 16 + N
430   LOCATE 6, 1
345   PRINT "INPUT";N;"ON PIN";PIN;"OF J";J;"IS CONNECTED TO TP1"
440   INPUT "PRESS RETURN TO CONTINUE", A$
445   NEXT N
450   CLS
455   PRINT "4b. TEST LOCAL MUX DIFFERENTIAL MODE"
460   FOR N= 0 TO 7
465   POKE CMDA, N
470   LOCATE 6, 1
475   PRINT "+INPUT";N;"ON PIN";9-N;"OF J1 IS CONNECTED TO TP1"
480   PRINT "- INPUT";N;"ON PIN";N+2;"OF J2 IS CONNECTED TO TP2"
485   INPUT "PRESS RETURN TO CONTINUE", A$
490   NEXT N
500   CLS
510   PRINT "5. TEST LOCAL AMP"
520   POKE CMDA, 0
530   PRINT "LOCAL GAIN = X1, 1 VOLT INPUT GIVES 1 VOLT OUTPUT AT TP3"
540   INPUT "PRESS RETURN TO CONTINUE", A$
550   CLS
560   POKE CMDA, 32
570   PRINT "LOCAL GAIN=X10, 1 VOLT INPUT GIVES 10 VOLT OUTPUT AT TP3"
580   INPUT "PRESS RETURN TO CONTINUE", A$
600   CLS
605   PRINT "6a. SETUP LOCAL AND GLOBAL AMP"
610   POKE CMDA, 0                          'SETUP LOCAL AMP
620   POKE CMDB, 1                          'SETUP GLOBAL INPUT AND AMP
630   PRINT "READ 1 VOLT AT PIN 28 OF U8"
635   INPUT "PRESS RETURN TO CONTINUE", A$
640   FOR N = 0 TO 3
650   CLS
655   PRINT "6b. TEST GLOBAL AMP"
660   POKE CMDB, 1 + (64 * N)               'SELECT GLOBAL GAIN
670   IF N < 2 THEN V=N+1 ELSE V=(N-1)*5 'DETERMINE VOLTAGE GAIN
680   PRINT "READ";V;"VOLTS AT TP9"
685   INPUT "PRESS RETURN TO CONTINUE", A$
690   NEXT N
700   POKE CMDA, 0                          'SELECT LOCAL AMP FOR 1V OUT
710   FOR N = 0 TO 15
```

```
715     CLS
720     PRINT "7.  TEST GLOBAL MUX"
730     LOCATE 6, 1
740     IF N < 8 THEN PIN = N + 19 ELSE PIN = 19 - N
750     POKE CMDB, N
760     IF N=0 OR N=14 THEN PRINT "0 VOLTS AT TP9"
765     IF N=1 THEN PRINT "1 VOLT FROM LOCAL AMP AT TP9"
770     IF N=13 THEN PRINT "10 VOLT REFERENCE AT TP9"
775     IF N=15 THEN PRINT "5 VOLT DIGITAL SUPPLY AT TP9"
780     IF N>1 AND N<13 THEN PRINT "SIGNAL AT PIN";PIN;"OF U8 AT TP9"
785     INPUT "PRESS RETURN TO CONTINUE", A$
790     NEXT N
800     CLS
810     PRINT "8.  TEST A/D CONVERTER"
820     POKE CMDA, 0                          'SETUP LOCAL AMP
830     POKE CMDB, 17                         'SETUP GLOBAL CHANNEL
840     POKE CMDD, 255                        'START CONVERSION
850     WHILE PEEK(CMDD) > 127: WEND          'WAIT FOR CONVERSION DONE
860     TOTAL=PEEK(CMDA) + PEEK(CMDB)*256  'GET READING, COMBINE
                                                              BYTES
870     VOLTS = TOTAL * 1.5259E-04            'CONVERT READING TO VOLTS
875     LOCATE 6,1
880     PRINT VOLTS
890     A$ = INKEY$
895     IF A$ = "" THEN GOTO 840
900     PRINT "TEST DONE"
910     END
```

AMM1A SPECIFICATIONS

INPUT CHANNELS

Local: 8 differential or 16 single-ended inputs.
Global: 9 inputs from slots 2-10.

LOCAL PROGRAMMABLE GAIN AMPLIFIER

Programmable Gains: x1, x10.
Gain Accuracy: ±0.045% @ x1 gain; ±0.08% @ x10 gain.
Nonlinearity: ±0.05%
Temperature Coeff: ±0.001%/°C @ x1 gain; ±0.0017%/°C @ x10 gain.
Input Resistance: >100MΩ.
Input Bias Current: <1nA.
Input Noise: <100µV p-p, 0.1Hz to 100kHz.
CMRR: >70dB, DC to 60Hz.
Input Protection: ±30V maximum (powered), ±15V maximum (unpowered).

10.000 VOLT REFERENCE

Accuracy: ±0.025%.
Temperature Coeff: ±0.0017%/°C.
Noise: 25µV p-p, 0.1Hz to 10Hz.

GLOBAL AMPLIFIER AND A-to-D CONVERTER

A-to-D Converter: Self-calibrating, successive approximation.
Resolution: 12-bits (1 part in 4,096).
A-to-D Range: Software selectable, 0 to +10V (unipolar) and -10V to +10V (bipolar).
Conversion Time: 16µsec. (including acquisition time).
Software Trigger:
- **Oneshot Mode:** A single reading is available 16µsec. after trigger location in memory is addressed.
- **Continuous Mode:** Conversions are continuously triggered every 16µsec. by internal crystal controlled clock.

External Gate: Continuous conversions begin with falling edge of input to J3 pin 2 and stop when input is high. TTL compatible.
Noise: <1/2 LSB on all ranges and gains.
Programmable Gains: x1, x2, x5, and x10.
Gain Accuracy*: ±(0.04% + 1 LSB) @ x1 gain; ±(0.15% + 1 LSB) @ x2, x5, and x10 gain.
Gain Nonlinearity*: ±0.033%.
Gain Temp. Coeff*: ±0.003%/°C.
Filter: Software selectable, 100kHz or 2kHz single pole.
Settling Time:** 12µsec. with 100kHz filter, 600µsec. with 2kHz filter.

*Includes input MUX, amplifiers, and A-to-D Errors.
**(to 0.05% of final reading)

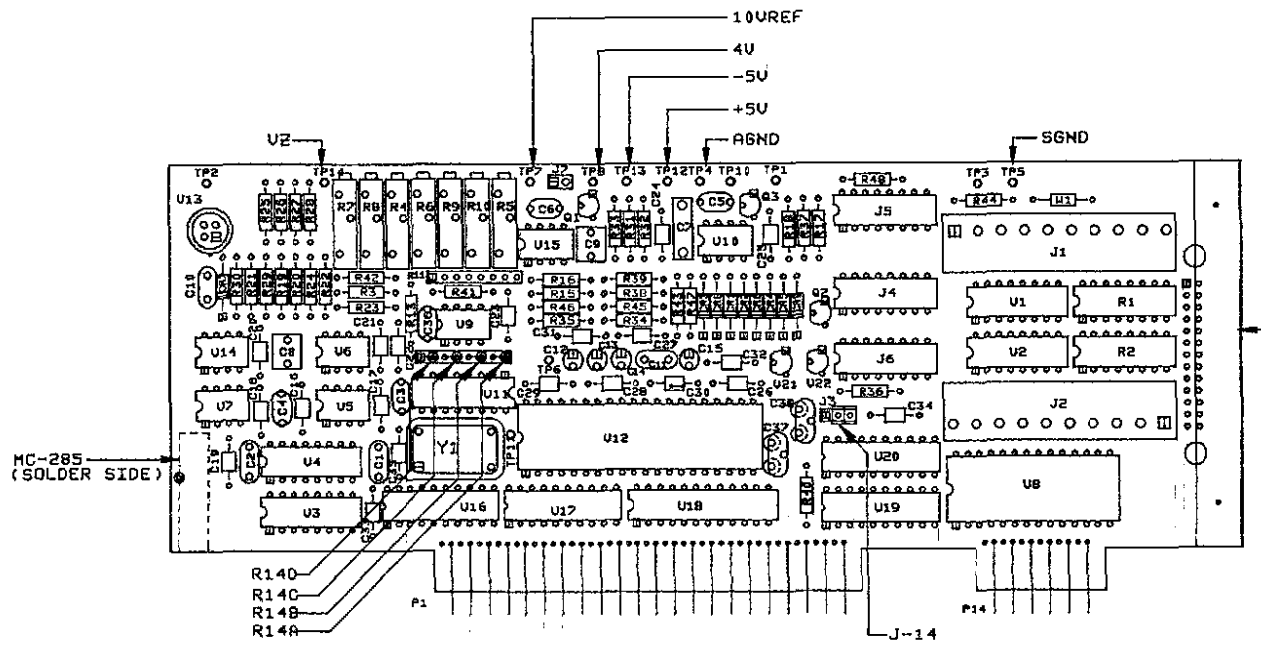
AMM1A PARTS LIST

PART NUMBER	TITLE	REMARKS
C-179-10	CAP, 10uF, 20%, 20V, TANTALUM	C12..C15
C-237-1	CAP, 1uF, 20%, 50V, CERAMIC	C10, C11
C-306-.001	CAP, 1000pF, 10%, 100V, POLYPROPYLENE	C7
C-350-1	CAP, 1uF, 20%, 50V, POLYESTER	C8, C9
C-365-.1	CAP,. 1uF, 20%, 50V CERAMIC	C16..C35
C-64-22P	CAP, 22pF, 10%, 1000V, CERAMIC	C1, C2, C36
C-64-10P	CAP, 10pF, 10%, 1000V, CERAMIC	C3, C4
C-64-100P	CAP, 100pF, 10%, 1000V, CERAMIC	C5
C-64-470P	CAP, 470pF, 10%, 1000V, CERAMIC	C6
CR-28-2	OSCILLATOR, 4 MHz	Y1
CS-339-4	CONN, 4-PIN	J3
CS-553	PIN, TEST POINT	TP1..TP14
CS-521-2	CONN, STRIP, 10 PIN	J1, J2
IC-607	IC, OCTAL BUS DRIVER, 74HCT541	U16, U17
IC-267	IC, 8 CH CMOS ANALOG MULTI, 6108	U1, U2, U11
IC-365	IC, 16 CHAN CMOS MULTIPLEXER, 6116	U8
IC-397	IC. OCTAL EDGE TRIG FLIP FLOP, 74HCT374	U19, U20
IC-603	IC, 5V VOLTAGE REGULATOR, 78L05	U21
IC-604	IC, -5V VOLTAGE REGULATOR, 79L05	U22
IC-674	IC, 12-BIT, A/D CONV, C55012	U12
IC-455	IC, DUAL SPST CMOS ANALOG SWITCH	U3, U4
IC-217	IC, VOLTAGE REFERENCE, LM399	U13
IC-176	IC, 18V, OP-AMP, LF351	U5..U7,U9,U10,U14,U15
IC-605	IC, PGMABLE LOGIC ARRAY, PAL20L10ACNS	U18
J-14	JUMPER	U18
SO-72	SOCKET, 8-PIN	FOR U18
SO-84-40	SOCKET, 40-PIN	FOR U12
SO-65	SOCKET, 16-PIN	FOR J4..J6,U18
CS-480	RESISTOR CARRIERS	J4..J6
R-263-10K	RES, 10K, .1%, 1/10W, METAL FILM	R41, R42,R14A
R-263-14.7K	RES, 14.7K, .1%, 1/10W, METAL FILM	R21
R-263-2.274K	RES, 2.274K, .1%, 1/10W, METAL FILM	R13
R-263-2.74K	RES, 2.74K, .1%, 1/10W, METAL FILM	R19
R-263-2.87K	RES, 2.87K, .1%, 1/10W, METAL FILM	R15
R-263-20K	RES, 20K, .1%, 1/10W, METAL FILM	R22
R-263-2K	RES, 2K, .1%, 1/10W, METAL FILM	R17, R14C,R14D
R-263-6.65K	RES, 6.65K, .1%, 1/10W, METAL FILM	R20
R-176-976	RES, 976, .1%, 1/8W, FIXED	R40
R-76-10	RES, 10, 5%, 1/4W, COMPOSITION OR FILM	R34, R35
R-76-100	RES, 100, 5%, 1/4W, COMPOSITION OR FILM	R32
R-76-22K	RES, 22K, 5%, 1/4W, COMPOSITION OR FILM	R38
R-76-390	RES, 390, 5%, 1/4W, COMPOSITION OR FILM	R33
R-76-47K	RES, 47K, 5%, 1/4W, COMPOSITION OR FILM	R36
R-76-5.6K	RES, 5.6K, 5%, 1/4W, COMPOSITION OR FILM	R39
R-76-8.2K	RES, 8.2K, 5%, 1/4W, COMPOSITION OR FILM	R31
R-263-6K	RES, 6K, .1%, 1/10W, METAL FILM	R14B
R-88-100K	RES, 100K, 1%, 1/8W, METAL FILM	R37
R-88-121	RES, 121, 1%, 1/8W, METAL FILM	R23

R-88-130	RES, 130, 1%, 1/8W, METAL FILM	R16
R-88-267K	RES, 267K, 1%, 1/8W, METAL FILM	R28
R-88-2K	RES, 2K, 1%, 1/8W, METAL FILM	R30
R-88-3.01K	RES, 3.01K, 1%, 1/8W, METAL FILM	R29
R-88-383K	RES, 383K, 1%, 1/8W, METAL FILM	R27
R-88-49.9K	RES, 49.9K, 1%, 1/8W, METAL FILM	R25
R-88-499	RES, 449, 1%, 1/8W, METAL FILM	R24
R-88-61.9K	RES, 61.9K, 1%, 1/8W, METAL FILM	R26
R-88-75K	RES, 75K, 1%, 1/8W, METAL FILM	R18
R-88-86.6K	RES, 86.6K, .1%, 1/8W, METAL FILM	R3
RF-28	DIODE, SILICON, IN4148 (DO-35)	CR1..CR9
RP-89-20K	POT, 20K, 10%, .75W, NON-WIREWOUND	R5, R6, R9,R10
RP-89-2K	POT, 2K, 10%, .75W, NON-WIREWOUND	R7, R8
RP-89-20K	POT, 20K, 10%, .75W, NON-WIREWOUND	R4
TF-175	RES NET, 10K, .01%, .1W	R11
TF-177-1	RES NET, 1K, 2%, 2.25W	R1, R2
TG-167	FET, TO-92 CASE	Q3
TG-47	TRANS, NPN SILICON, 2N3904 (TO-92)	Q1
TG-84	TRANS, PNP SILICON, 2N3906 (TO-92)	Q2

NO. 501-190

LTR.	ECO NO.	REVISION	ENG.	DATE
B	12649	RELEASED	SZ	2-9-88
B1	12780	RE-LABEL TP,ADDED J-14,C36	SZ	5-9-88
C	13248	REVISED	SZ	4-7-89
D	13562	ARTWORK WAS REV.C	SZ	6-26-89
D1	13595	ADDED (1) MC-285	SZ	8-8-89
E	14357	ARTWORK WAS REV D-ADDED CSP & C38-CHG'D R34 FROM R34-17K TO R34-1.7K & CS FROM TP-24 TO TP-19).	AS	1-14-91
E1	14663	CHG'D TESTPOINTS FROM CS-553 TO CS-463		7-16-91
F	14787	ARTWORK WAS REV.E	dd	1-17-92

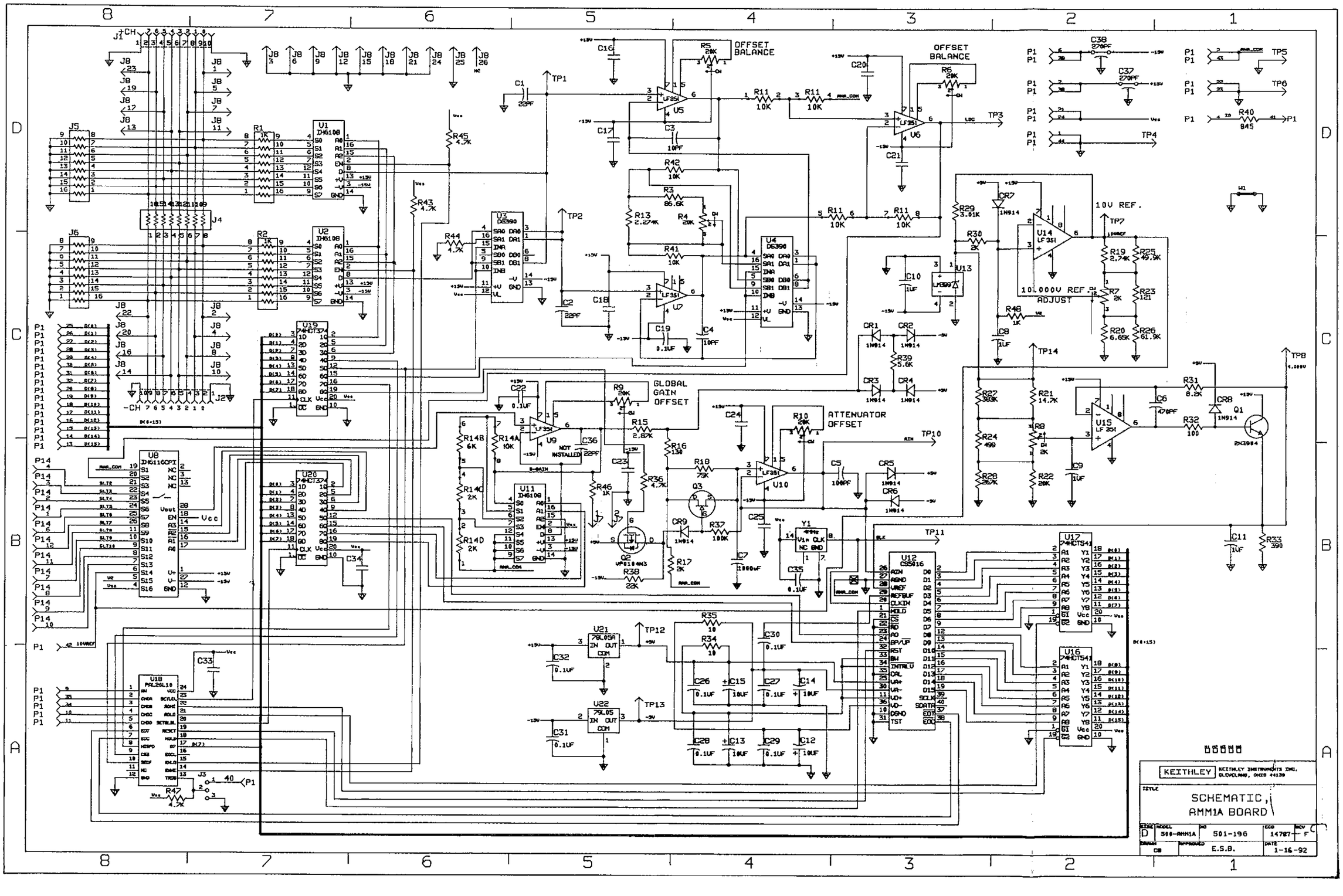


NOTE:
DO NOT INSTALL C36.

NOTE:
FOR COMPONENT INFORMATION, REFER TO BILL OF MATERIAL (501-977).

AMM1A		
MODEL	NEXT ASSEMBLY	QTY.
USED ON		

DO NOT SCALE THIS DRAWING	DIMENSIONAL TOLERANCES UNLESS OTHERWISE SPECIFIED	DATE 12-2-88	SCALE 1:1	TITLE COMPONENT LAYOUT, AMM1A
	XX=±.015 ANG.=±1°	DRN. CB	ENG. APPR. MS	
KEITHLEY KEITHLEY INSTRUMENTS INC. CLEVELAND, OHIO 44139	XXX=±.005 FRAC.=±1/64	MATERIAL	C	NO. 501-190
	SURFACE MAX. 63	FINISH		


OFFSET BALANCE
OFFSET BALANCE
GLOBAL GAIN OFFSET
ATTENUATOR OFFSET
10V REF.
10.000V REF ADJUST
SCHEMATIC, AMM1A BOARD
KEITHLEY
KEITHLEY INSTRUMENTS INC.
CLEVELAND, OHIO 44139
MODEL 500-AMM1A
NO 501-196
ECO 14787
REV F
DRAWN CB
APPROVED E.S.B.
DATE 1-16-92